YieldStar Metrology System Applications for Advanced Process Control

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Overlay and CD-Uniformity (CDU) are critical for device performance.

Today’s devices: CD ≈ 16 nm
OV < 5 nm
CDU < 1.5 nm

Rule-of-thumb:
OV ≈ 30 % of CD
CDU ≈ 10 % of CD
ASML Holistic Lithography approach seeks to maximize patterning process performance and control

1. Lithography scanner with advanced capability (Imaging, overlay and focus)

2. Process Window Control

3. Computational Lithography

Full chip process window detection

Metrology
YieldStar Optical Scatterometry System
Overlay, Focus and CD measurement capability

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Signal type</th>
<th>Target size (µm²)</th>
<th>Primary application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overlay After Develop</td>
<td>Pupil</td>
<td>40x160</td>
<td>Monitor wafer</td>
</tr>
<tr>
<td></td>
<td>Dark field image</td>
<td>10x10</td>
<td>On Product</td>
</tr>
<tr>
<td>Focus</td>
<td>Pupil</td>
<td>40x80</td>
<td>Monitor wafer</td>
</tr>
<tr>
<td></td>
<td>Dark field image</td>
<td>10x10</td>
<td>On Product</td>
</tr>
<tr>
<td>CD &amp; Overlay At Resolution</td>
<td>Pupil</td>
<td>40x40 – 5x5</td>
<td>Monitor &amp; On Product</td>
</tr>
</tbody>
</table>
After develop measurements with YieldStar
Design for Control optimizes YieldStar overlay targets for best on-product overlay performance

**Printability**
- Mask optimization
- Litho process window
- Design rule compatibility

**Detectability**
- Optimize precision (TMU) and measurement time (MAM)
- Dependent on stack & target design

**Process robustness**
- Measurement robust for process variations (detectability & accuracy)

**Device matching**
- Aberration sensitivity
- Match target to device

\[
\frac{\partial OVL_d}{\partial Z_i} \approx \frac{\partial OVL_t}{\partial Z_i}
\]
YieldStar Dark Field (μDBO) Measurement Principle
YS350 allows parallel detection of + and – first order image

YieldStar Image of μDBO target on the wafer

\[ A^+ = I^{(+1\text{st})}_{+d} - I^{(-1\text{st})}_{+d} \]

\[ A^- = I^{(+1\text{st})}_{-d} - I^{(-1\text{st})}_{-d} \]

\[ OV = d \times \frac{A^+ + A^-}{A^+ - A^-} \]

\( A \) is asymmetry (delta Intensity)
\( A^+ = K(OV + d) \)
\( A^- = K(OV - d) \)
\( K \) is overlay sensitivity
\( d \) is grating bias

μDBO target on the wafer
Overlay recipe optimization required

Presence of grating asymmetry, imbalance along with film variations trigger an overlay swing phenomena

In the absence of asymmetry → life is easy in OV metrology

But when asymmetry is present, each measurement site may be susceptible to an OV error which will vary with the variation of …

1. Asymmetry over wafer
2. Field location specific grating imbalance
3. Symmetric stack parameters (thin film thickness etc.) over the wafer
4. Any or all of the above from W2W, L2L

Goal is to eliminate or minimize these errors
Multi Wavelength approach towards accuracy & robustness

Enabled by continuous WL and fast WL switching hardware (reducing throughput penalty)

DBO uses overlapping gratings with a shift (bias) +d and -d

\[ A^+ = K(OV + d) \quad A^- = K(OV - d) \]

\( A^+ = \left( \frac{OV+d}{OV-d} \right) A^- \)

Each colored dot is a different WL

Every WL has the same slope to origin = same OV

Symmetric gratings

Asymmetric gratings

\[ A^+ = \left( \frac{OV+d}{OV-d} \right) A^- + C \]

Every WL has different slope to origin = wrong OV

Distance to origin (DTO) = measure of asymmetry ~ C

Slope is proportional to overlay in \( A^+ \) vs. \( A^- \) plot

Multi WL (at least dual WL) can describe the OV more accurately than 1 WL

Slope of multi WL line immune to asymmetry = accurate OV

\( K \) is overlay sensitivity: detects process dependency of overlay

\( A \) is asymmetry (delta intensity)
Simulation showing the robustness of Dual WL

Result of Monte-Carlo simulation

4 stack parameters were randomly varied:

1. Oxide film thickness: 390 – 410 nm
2. Grating imbalance: 2 nm top-top
3. Side wall asymmetry: ± 1 nm impact
4. Etch depth: 77 – 83 nm

For 140 random selections the OV error was calculated for the single wavelength and the dual wavelength recipe:

Dual WL remains immune to large stack variations
Single WL doesn’t match to AEI device OV (reference)  
Multi WL can bring the result closer to the reference

<table>
<thead>
<tr>
<th>ADI YieldStar Single Wavelength Recipes</th>
<th>ADI YieldStar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wavelength 1</td>
<td></td>
</tr>
<tr>
<td>Wavelength 2</td>
<td></td>
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<tr>
<td>Wavelength 3</td>
<td></td>
</tr>
<tr>
<td>Wavelength 4</td>
<td></td>
</tr>
<tr>
<td>AEI Reference</td>
<td>Reference</td>
</tr>
<tr>
<td>Multi WL</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Overlay</th>
<th>Wavelength 1</th>
<th>0.69</th>
<th>Wavelength 2</th>
<th>0.74</th>
<th>Wavelength 3</th>
<th>0.86</th>
<th>Wavelength 4</th>
<th>0.95</th>
<th>AEI Reference</th>
<th>Slope = 0.98</th>
<th>Multi WL</th>
</tr>
</thead>
</table>

Correlation Slope to AEI Reference (critical x dir)

- Overlay
- All R2 are > 0.95

All measurement WLs are used to create the Multi WL result above
Dual & multi WL OV not impacted by asymmetry induced error

Single WL OV (even @ signal peaks) do not match reference, but multi WL (and also dual WL) provide good match to reference OV

Assuming
1. the error sources not related to asymmetry are excluded by target design
2. no etch (post ADI) induced ADI to AEI delta
Dual WL showing better accuracy and lot to lot overlay robustness compared to single WL measurements

A reduction of 40% lot to lot non-correctable error (NCE) is observed below indicating less systematic error present in dual WL compared to single WL.
After etch measurements with YieldStar In Device Metrology (IDM)
Litho Overlay Metrology on Target to After Etch
Device offsets are a common problem today in HVM

<table>
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<tr>
<th>ADI Litho – uDBO Overlay</th>
<th>Zero Overlay</th>
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</thead>
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<tr>
<td>AEI-ADI offset</td>
<td></td>
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</table>

<table>
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<tr>
<th>After Etch – Cell Overlay</th>
<th>Zero Overlay</th>
</tr>
</thead>
<tbody>
<tr>
<td>AEI-ADI offset</td>
<td></td>
</tr>
</tbody>
</table>
In-Device Metrology (IDM) Overlay: Concept

When both OV gratings are in close proximity, the resulting OV-induced 0th-Order Pupil Asymmetry signals can be exploited.

Overlay Principle

Overlay Metrology

Overlay asymmetry signal fully captured with YieldStar’s unique design within one acquisition.
In-Device Metrology (IDM) enables accurate and dense overlay metrology on device level features. IDM measures allows flexible sampling and High Order corrections.

Typical μDBO Targets
Scribelane based

<30 points per field

YS1375 Enable Overlay and μCD DRAM features

>1000 points per field

<table>
<thead>
<tr>
<th>Field Coverage</th>
<th>Scribelane ONLY (2% Reticle)</th>
<th>In-Device Full Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Flexibility</td>
<td>Limited</td>
<td>Full</td>
</tr>
<tr>
<td>Matched to Device Overlay</td>
<td>600nm Pitch Target</td>
<td>Device</td>
</tr>
</tbody>
</table>
YieldStar S1250 shows similar overlay fingerprints to CDSEM Overlay with 98% accuracy with respect to induced overlay.

**Set/Get Overlay +/-5.2nm**

98% Yieldstar Accuracy (Slope)

**Interfield Fingerprint**

Similar Interfield Fingerprint

**Intrafield Fingerprint**

Similar Intrafield Fingerprint

**Measurement Statistics**

YieldStar S1250 shows similar overlay fingerprints to CDSEM Overlay with 98% accuracy with respect to induced overlay.

**Set OV Range +/-5.2nm**

**CDSEM/DECAP**

**Intrafield**

IDM Intrafield

**CDSEM Intrafield**

**MAM Time**

0.5 sec

**Precision**

0.087 nm 3σ
In-Device Metrology (IDM) enables accurate and dense overlay metrology on device level features. IDM measures allows flexible sampling and High Order corrections.

**Typical μDBO Targets**
- Scribelane based
- <30 points per field

**Device Pitch**
- 600nm
- 10x10μm² targets

**Field Coverage**
- Scribelane ONLY (2% Reticle)

**Sampling Flexibility**
- Limited

**Matched to Device Overlay**
- 600nm Pitch Target

**YS1375 Enable Overlay and μCD DRAM features**
- >1000 points per field

**In-Device Full Field**
- Full
- Device

**YS 1250/1375 Enable Overlay and μCD logic features**
- >150 points per field

**In-Device Targets >90%**
- Maximized
- Device Feature
IDM needs target design for logic

Logic SRAM features can be simplified to enable fast and reliable metrology

Product Layout (up to contact layer)

Extract Layers of Interest
Define Overlay parameters

Contact to Gate

IDM target
Point symmetric unit cell

SYMMETRY RULES

- Point symmetry for geometry and materials
- The Point symmetry is broken in presence of Overlay

PITCH RULES

- Pitch as close as possible to product pitch
Small device-like targets correlate well with larger scribelane targets

$5 \times 5 \mu m^2$ and $10 \times 10 \mu m^2$ optimized IDM recipes show consistent behavior

<table>
<thead>
<tr>
<th>IDM target</th>
<th>Slope</th>
<th>$R^2$</th>
<th>Offset</th>
<th>Precision</th>
</tr>
</thead>
<tbody>
<tr>
<td>$10 \times 10 \mu m^2$</td>
<td>1.0</td>
<td>0.93</td>
<td>-0.53nm</td>
<td>0.10nm</td>
</tr>
<tr>
<td>$5 \times 5 \mu m^2$</td>
<td>0.97</td>
<td>0.91</td>
<td>-0.64nm</td>
<td>0.37nm</td>
</tr>
</tbody>
</table>
YieldStar IDM used to measure dense overlay fingerprint

- **DRAM (device)**
  - Get overlay [nm]
  - Slope = 0.98
  - $R^2 = 0.98$
  - 0.5 s MAM time
  - 164 points per field
  - Overlay data proprietary

- **Logic (5x5 $\mu$m$^2$ target)**
  - Get overlay [nm]
  - Slope = 0.97
  - $R^2 = 0.91$
  - 1.8 s MAM time
  - 145 points per field

Overlay Residuals

- Mean + 3$\sigma$ = 3.8 nm
- Mean + 3$\sigma$ = 2.2 nm
- 59% reduced

19 par/field CPE correction per exposure
>36% Device overlay improvements on DRAM word line with implementation of YieldStar In Device Metrology

<table>
<thead>
<tr>
<th>Controlling Metrology Tool</th>
<th>High Voltage SEM</th>
<th>Yieldstar IDM</th>
<th>Yieldstar IDM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Frequency</td>
<td>Low (Static)</td>
<td>Low (Static)</td>
<td>High</td>
</tr>
<tr>
<td>Lot Sampling Rate</td>
<td>Low</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Wafer Sampling Points</td>
<td>Low</td>
<td>High</td>
<td>High</td>
</tr>
</tbody>
</table>

![Graph showing device overlay control with Mean 3σ [nm] and data points for 11 months, 8 months, and 5 months. The graph illustrates a total improvement of 36% with YieldStar IDM.]

- **27%↓**
- **Total 36%↓**
IDM \( \mu \text{CD} \) measurements on 5x5 \( \mu \text{m}^2 \) match 10x10 \( \mu \text{m}^2 \)

*After-Etch Across Wafer*

**Target:** test target

**Sampling:** full wafer, 16 pts per field

**Results:**
- Good correlation of full wafer CD
- Clear etch process fingerprint
- Same residuals
Summary

- Combination of integrated and stand-alone metrology to support Scanner-stability and process-variation control.

- Overlay capability on optimized targets for good printability, low process sensitivity, high detectability, good matching to device.

- Multi-WL recipes required to meet accuracy requirements

- 5x5μm² target At Resolution OV and CD capability allows high density Intra- and Intra- field fingerprint metrology for improved after etch patterning control.